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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,641	02/02/2004	Taek-Seung Kim	51876P590	1582

8791 7590 07/29/2005

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,641	KIM, TAEK-SEUNG	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,10 and 11* is/are rejected.

7)☒ Claim(s) *3 and 6-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search Hisoty*.

DETAILED ACTION

1. This office action acknowledges receipt of the following items from the Applicant:

The Specification, Claims, Abstract, and Drawings filed on 02 February 2004.

Oath or Declaration filed on 07 July 2004.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in 10/770641 on 02 February 2004. It is noted, however, that applicant has not filed a certified copy of the Republic of Korea 2003-86257 application as required by 35 U.S.C. 119(b).

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because it uses the phrase **"semiconductor memory device includes"** in lines 1-2, which is implied. Correction is required. See MPEP § 608.01(b).

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. The disclosure is objected to because of the following informalities:

In line 3-4, paragraph 0029: Please replace "a second input NMOS transistor **M23**" with "a second input NMOS transistor **M22**".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 4-5 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (US. 6,636,443) in view of Jeong et al. (US. 6,192,429).

For the purpose of this rejection, the differential amplifying such as an input of NMOS transistors (transistor M12, M22 whose gate receives the address signal **AIN** and transistor M13, M23 whose gate receive the reference voltage **Vref**) as shown in the specification in paragraph 0008 and paragraph 0029.

Regarding independent claim 1, Kang in Fig. 4 and Fig. 13 discloses an address input buffer (340, Fig. 4) in a semiconductor memory device (a state machine of SDRAM in Fig. 4, see column 4, lines 23-24) comprising:

a differential amplifying (two NMOS transistor which is the first NMOS transistor have the gate receive the reference voltage (Vref) and the second MOS transistor have the gate receive the address signal (Pad) shown in Fig. 13) for differential amplifying a reference voltage (Vref) and an external address signal (Pad) (see column 4, lines 31-34 and column 6, lines 35-45).

Kang fails to explicitly mention a controlling for controlling the differential amplifying by receiving a refresh signal and a bank active signal.

Jeong et al., for example, discloses a controller (25, Fig. 2) for controlling the differential amplifying receive a refresh signal (RFS, Fig. 2) and a bank active signal (PRAL, Fig. 2, the controller 25 activates the enable signal EN only when at least one of active signal PRAL to generate output to memory array 23 such as bank) (see column 4, lines 22-28).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kang by incorporating the provide of Jeong for using the controller preferably enable/disable the current source during a row active period of the read/write operation and during latency period of the read/write operation of memory device (see column 3, lines 45-51).

With respected to dependent claim 2, Kang in view of Jeong et al. discloses an address input buffer in a semiconductor memory device as in independent claim 1 above. Jeong et al. further disclosed the controlling receive a power down signal (PWD, Fig. 2).

Since Kang and Jeong et al. are both in the same field of endeavor, the purpose disclosed by Jeong et al. would have been recognized in the pertinent art of Kang.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kang by incorporating the provide of Jeong for using the controller preferably the power down signal for activate the logic of enable/disable of the data input/output buffer in the integrated circuit (see column 2, lines 35-39).

For the purpose of this rejection, the differential amplifying such as an input of NMOS transistors (transistor M12, M22 whose gate receives the address signal **AIN** and transistor M13, M23 whose gate receive the reference voltage **Vref**) as shown in

the specification in paragraph 0008 and paragraph 0029; and the current mirror such as PMOS transistor (transistor M14, M15, M24, M25 being connected between a power supply) as shown in the specification in paragraph 0008 and paragraph 0029.

Regarding independent claim 4, Kang in Fig. 4 and Fig. 13 discloses an address input buffer (340, Fig. 4) in a semiconductor memory device (a state machine of SDRAM in Fig. 4, see column 4, lines 23-24) comprising:

a differential amplifying (two NMOS transistor which is the first NMOS transistor have the gate receive the reference voltage (Vref) and the second MOS transistor have the gate receive the address signal (Pad) shown in Fig. 13) for differential amplifying a reference voltage (Vref) and an external address signal (Pad) (see column 4, lines 31-34 and column 6, lines 35-45)

a current mirroring (gate of two PMOS transistor connected source and drain of NMOS transistor which the NMOS gate connected to power supply in Fig. 13) unit connect between the differential input (NMOS transistor which gate receive input Vref and NMOS transistor which gate receive input Pad) unit and a first voltage;

a biasing (NMOS transistor which gate receive input CKE, Fig. 3) unit which is connected between the differential input (NMOS transistor which gate receive input Vref and NMOS transistor which gate receive input Pad) and a second voltage for supplying bias current to the differential input and the current mirror (gate of two PMOS transistor connected source and drain of NMOS transistor which the NMOS gate connected to power supply in Fig. 13).

Kang fails to explicitly mention a controlling unit for enable/disable the bias unit by receiving a refresh signal and a bank active signal.

Jeong et al., for example, discloses a controller (25, Fig. 2) for controlling the bias unit for receive a refresh signal (RFS, Fig. 2) and a bank active signal (PRAL, Fig. 2, the controller 25 activates the enable signal EN only when at least one of active signal PRAL to generate output to memory array 23 such as bank) (see column 4, lines 22-28).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kang by incorporating the provide of Jeong for using the controller preferably enable/disable the current source during a row active period of the read/write operation and during latency period of the read/write operation of memory device (see column 3, lines 45-51).

With respected to dependent claim 5, Kang in view of Jeong et al. discloses an address input buffer in a semiconductor memory device as in independent claim 4 above. Jeong et al. further disclosed the controlling receive a power down signal (PWD, Fig. 2).

Since Kang and Jeong et al. are both in the same field of endeavor, the purpose disclosed by Jeong et al. would have been recognized in the pertinent art of Kang.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kang by incorporating the provide of Jeong for using the controller preferably the power down signal for activate the logic

of enable/disable of the data input/output buffer in the integrated circuit (see column 2, lines 35-39).

With respected to dependent claim 10, Kang in view of Jeong et al. discloses an address input buffer in a semiconductor memory device as in independent claim 4 and dependent claim 5 as above. Kang. further disclosed the an address input buffer comprising a CMOS inverter (inherence, the cmos inverter is static of NMOS and PMOS shown in Fig. 13) connected to an output node provided in the differential input unit.

Since Kang and Jeong et al. are both in the same field of endeavor, the purpose disclosed by Jeong et al. would have been recognized in the pertinent art of Kang.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kang and Jeong using CMOS as PMOS and NMOS transistors wired together in a balanced fashion that causes less power to be used than NMOS or PMOS transistors by themselves in the device.

For the purpose of this rejection. The precharge unit as described in the specification in paragraph 0036 such as PMOS transistor M26, M27 are turn on to thereby precharge the output node would consider same as two PMOS transistor Fig. 13 which both two PMOS transistor have gate connected to CKE of reference Kang for the precharge unit.

With respected to dependent claim 11, Kang in view of Jeong et al. discloses an address input buffer in a semiconductor memory device as in independent claim 4 and

dependent claim 5 as above. Kang. further disclosed the precharge unit (two PMOS transistor shown in Fig. 13 which is both gates connected to clock (CKE) generate the input gate bias transistor) for precharging the output node (D1) in response to an output signal of the controlling unit.

Since Kang and Jeong et al. are both in the same field of endeavor, the purpose disclosed by Jeong et al. would have been recognized in the pertinent art of Kang.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kang and Jeong using precharge unit for comparing the command signal and reference voltage to the output in the address input buffer of a semiconductor device.

Allowable Subject Matter

9. Claims 3 and 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 3 and 6, the prior art of record do not disclose or suggest an inverter receiving an output of the Nand gate and a Nor gate receiving an output of the inverter and the power down signal of an address buffer of a semiconductor memory device.

Regarding claim 8, the prior art of record do not disclose or suggest a Nor gate receiving an output of the inverter, the power down signal and a second inverter receiving an output of the Nor gate in an address buffer in a semiconductor memory device.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

pL

PML
July 18 2005